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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/241,177	02/01/99	AKRAM S	3638US-(98-0

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JAMES R DUZAN
TRASK BRITT & ROSSA
P O BOX 2550
SALT LAKE CITY UT 84110

EXAMINER	
NOVACEK,C	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/241,177	AKRAM ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) *1-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 1999 and 03 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

DETAILED ACTION

This Office Action is in response to the communication filed February 1, 1999.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-31, drawn to a semiconductor device, classified in class 257, subclass 690.

II. Claims 32-55, drawn to a method of making a semiconductor device, classified in class 438, subclass 106.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as made can be made by a materially different process. For example, the semiconductor device, as disclosed in claims 1-31, could have the semiconductor die placed in any pattern on the substrate, as long as at least one die is bonded to the first side of the substrate and aligned with a through-slot and one other die is bonded to the second side of the substrate and aligned with a through-slot. The method of making a semiconductor device, as disclosed in claims 32-55, requires that die on one side of the substrate are aligned with alternate through-slots while the die on the other side of the substrate are aligned with other alternate through-slots.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. James Duzan on May 14, 2001 a provisional election was made without traverse to prosecute the invention of Group II, claims 32-55. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1-31 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Reference sign "32", as stated on page 7, lines 2, 12 and 14, page 9, lines 21 and 23, and page 10, line 4 of the specification.

Reference sign "30" as stated on page 9, lines 14, 21 and 24, and page 10, lines 6, 10 and 16 of the specification.

Reference sign "35" as stated on page 9, line 20 of the specification.

Correction is required.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because Figure 10 as well as substitute Figure 9 shows the reference sign "30B" pointing to the middle through-slot and reference sign "30C" pointing to one of the outer through-slots, while Figures 3, 5 and 6,

as well as the specification on page 6, line 28-page 7, line 4, disclose that the middle through-slot is designated as "30C" and the outer through-slots are labeled "30A" and "30B". Correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 35-37 and 47-49 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 35 and 47 recite the limitation of a "flowable hardenable glob-top material". This limitation is not supported by the specification which does not disclose the glob-top material to be "flowable" or "hardenable". Claims 36 and 48 recite the limitations of a "hardenable polymeric material". The specification does not disclose the polymeric material to be "hardenable". Claims 37 and 49 are rejected for their dependence upon claims 35-36 and 47-48, respectively.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 32-55 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as

and second sides (92, 94) and at least three elongate through-slots (86) extending from the first side to the second side. A pattern of conduits (118) (inherently electrical conductors) connected to terminal contacts (82) are adjacent to the through-slots on the substrate. The terminal contacts connect the bond pads of the dice the conduits which, in turn, connect to an input/output connector (104). The active surface of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surface of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 1 and 2 and col. 4, ln. 37-63.

In reference to claim 33, the through-slots are made by forming an elongate stepped surface in the through-slots (Fig. 2-4).

In reference to claim 34, conductive connection terminals are formed on the elongate stepped surface (Fig. 3-4).

In reference to claim 35, a glob-top material (90) is inserted into each through-slot to encapsulate the wires (Fig. 1; col. 5, ln. 49-59). This material is disclosed to be a resin which is, inherently, flowable and hardenable.

In reference to claim 36, a hardenable polymeric material is inserted into each through-slot (Fig. 1; col. 5, ln. 49-59).

In reference to claim 37, as can been seen in Figure 1, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

the invention. Lines 7-9 of claims 32 and 42 are unclear as written. It is not understood what is meant by "configured for opposite side access between attached semiconductor dice...and the plurality of bond pads". Claims 33-43 and 45-55 are rejected for their dependence upon claims 32 and 44 respectively.

Claim Objections

Claim 43 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 42 recites the limitation of having an input/output connector comprising either a ball-grid array or a pin-grid array. Claim 43, which depends upon claim 42, recites the limitation of the input/output connector comprising a socket connector.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

1. Claims 32-37, 39-40, 44-49 and 51-52 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al.

In reference to claim 32, Chan discloses a plurality of semiconductor dice (50) each having an active surface and a plurality of bond pads (120). A substrate (70) has opposing first

In reference to claim 39, the polymeric material described above in reference to claim 36 is also used to encapsulate/seal the die (Fig. 1 and 5; col. 6, ln. 54-58).

In reference to claim 40, the step of forming a pattern of electrical conductors includes forming a conductor pattern on the first and second sides of the substrate (Fig. 1 and 2; col. 4, ln. 58-67).

In reference to claim 44, Chan discloses a plurality of integrated circuit dice (50) each having an active surface and a row of conductive bond pads (120). A planar substrate (70) has opposing first and second sides (92, 94) and at least three elongate through-slots (86) extending from the first side to the second side. A pattern of conduits (118) (inherently electrical conductors) connected to terminal contacts (82) are adjacent to the through-slots on the substrate. The terminal contacts connect the bond pads of the dice the conduits which, in turn, connect to an input/output connector (104). The active surface of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surface of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the corresponding through-slots. See Fig. 1 and 2 and col. 4, ln. 37-63.

In reference to claim 45, the through-slots are made by forming an elongate stepped surface in each through-slots (Fig. 2-4).

In reference to claim 46, conductive connection terminals are formed on the elongate stepped surface (Fig. 3-4).

In reference to claim 47, a glob-top material (90) is inserted into each through-slot to encapsulate the wires (Fig. 1; col. 5, ln. 49-59). This material is disclosed to be a resin which is, inherently, flowable and hardenable.

In reference to claim 48, a hardenable polymeric material is inserted into each through-slot (Fig. 1; col. 5, ln. 49-59).

In reference to claim 49, as can been seen in Figure 1, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claim 51, the polymeric material described above in reference to claim 48 is also used to encapsulate/seal the die (Fig. 1 and 5; col. 6, ln. 54-58).

In reference to claim 52, the step of forming a pattern of electrical conductors includes forming a conductor pattern on the first and second sides of the substrate (Fig. 1 and 2; col. 4, ln. 58-67).

Claim Rejections - 35 USC § 102/103

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 32, 38, 40, 44, 50 and 52 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Chiu.

In reference to claim 32, Chiu discloses a plurality of semiconductor dice (32) each having an active surface and a plurality of bond pads (35). A substrate (31) has opposing first and second sides and at least three elongate through-slots (33) extending from the first side to the second side. A pattern of circuitry (inherently electrical conductors) connected to terminal contacts (34) are adjacent to the through-slots on the substrate (col. 2, ln. 2-9). The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surface of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the through-slots. See Fig. 3-5 and col. 2, ln. 2-9 and ln. 33-47. Chiu does not disclose the circuit board (substrate) to have an input/output connector. However, the circuit board must inherently have an input/output connector so that the semiconductor dice can be electrically accessed by the hardware that it is connected to. Similarly, the input/output connector must also inherently be connected to the terminal contacts (34) in order to be electrically connected to the dice. In the alternative, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to form the inherent input/output connector such that it is connected to the terminal contacts because the terminal contacts are connected to the semiconductor dice which must be connected to an electrical source in order to function.

In reference to claim 38, the semiconductor dice is electrically tested following wire-bonding but prior to wire encapsulation (col. 2, ln. 31-32).

In reference to claim 40, Chiu discloses forming a pattern of circuitry (electrical conductors) on the circuit board (substrate) but does not specifically disclose forming a conductor pattern on both the first and second sides of the board (col. 2, ln. 7-15). However, according to Chiu, a short bond wire connects each semiconductor die on both sides of the substrate to the circuitry on the circuit board. This would inherently require a pattern of circuitry to be on both sides of the board.

In reference to claim 44, Chiu discloses a plurality of integrated circuit dice (32) each having an active surface and a row of conductive bond pads (35). A planar substrate (31) has opposing first and second sides and at least three elongate through-slots (33) extending from the first side to the second side. A pattern of circuitry (inherently electrical conductors) connected to terminal contacts (34) are adjacent to the through-slots on the substrate (col. 2, ln. 2-9). The active surfaces of some of the dice are attached to the first side of the substrate and the bond pads of the dice are aligned with alternate through-slots for access from the second side of the substrate. The active surface of some of the other dice are attached to the second side of the substrate and the bond pads of these dice are also aligned with alternate through-slots for access from the first side of the substrate. The bond pads of the dice are wire-bonded to the terminal contacts adjacent the corresponding through-slots. See Fig. 3-5 and col. 2, ln. 2-9 and ln. 33-47. Chiu does not disclose the circuit board (substrate) to have an input/output connector. However, the circuit board must inherently have an input/output connector so that the semiconductor dice can be electrically accessed by the hardware that it is connected to. Similarly, the input/output

connector must also inherently be connected to the terminal contacts (34) in order to be electrically connected to the dice. In the alternative, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to form the inherent input/output connector such that it is connected to the terminal contacts because the terminal contacts are connected to the semiconductor dice which must be connected to an electrical source in order to function.

In reference to claim 50, the semiconductor dice is electrically tested following wire-bonding but prior to wire encapsulation (col. 2, ln. 31-32).

In reference to claim 52, Chiu discloses forming a pattern of circuitry (electrical conductors) on the circuit board (substrate) but does not specifically disclose forming a conductor pattern on both the first and second sides of the board (col. 2, ln. 7-15). However, according to Chiu, a short bond wire connects each semiconductor die on both sides of the substrate to the circuitry on the circuit board. This would inherently require a pattern of circuitry to be on both sides of the board.

Claim Rejections - 35 USC §103

1. Claims 35-37, 39, 47-49 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Chan et al.

In reference to claims 35 and 36, a glob-top material (36) is inserted into each through-slot to encapsulate the wires (Fig. 4; col. 2, ln. 31-32). Chiu does not disclose what type of encapsulant is used. However, it is well known in the art to use a flowable, hardenable polymeric material, such as a resin, to encapsulate wires in an integrated circuit package, as is shown by the invention of Chan (Fig. 1; col. 5, ln. 49-59). At the time of the invention, it would

have been obvious to one of ordinary skill in the art to use a hardenable, flowable polymeric material, such as a resin, to encapsulate the wires of Chiu because it is well known and conventional practice in the art to use an encapsulant that is flowable so that the material can completely surround and seal the wires while also being hardenable so that it can protect the wires from subsequent processing.

In reference to claim 37, as can been seen in Figure 4, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claim 39, Chiu discloses encapsulating the wires but not the semiconductor dice (Fig. 4; col. 2, ln. 31-32). Chan's IC package has both the semiconductor dice and the wires encapsulated to hermetically protect them from moisture (Fig. 1 and 5, col. 6, ln. 54-58; col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to encapsulate the dice of Chiu in addition to the wires because, as is well known in the art, semiconductor dice can be fatally damaged by moisture and by encapsulating them, the dice can be protected against malfunction.

In reference to claims 47 and 48, a glob-top material (36) is inserted into each through-slot to encapsulate the wires (Fig. 4; col. 2, ln. 31-32). Chiu does not disclose what type of encapsulant is used. However, it is well known in the art to use a flowable, hardenable polymeric material, such as a resin, to encapsulate wires in an integrated circuit package, as is shown by the invention of Chan (Fig. 1; col. 5, ln. 49-59). At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a hardenable, flowable polymeric material, such as a resin, to encapsulate the wires of Chiu because it is well known and conventional practice in the art to use an encapsulant that is flowable so that the material can

completely surround and seal the wires while also being hardenable so that it can protect the wires from subsequent processing.

In reference to claim 49, as can been seen in Figure 4, the glob-top material is inserted to extend outwardly between the edges of at least two die proximate each side of the through-slots.

In reference to claim 51, Chiu discloses encapsulating the wires but not the semiconductor dice (Fig. 4; col. 2, ln. 31-32). Chan's IC package has both the semiconductor dice and the wires encapsulated to hermetically protect them from moisture (Fig. 1 and 5, col. 6, ln. 54-58; col. 7, ln. 33-35). At the time of the invention, it would have been obvious to one of ordinary skill in the art to encapsulate the dice of Chiu in addition to the wires because, as is well known in the art, semiconductor dice can be fatally damaged by moisture and by encapsulating them, the dice can be protected against malfunction.

2. Claims 41 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Swamy et al.

Chiu shows in Figure 4 that the dice mounted to the first side of the circuit board are electrically connected to the surface of the second side of the circuit board by wires. The dice mounted to the second side of the circuit board are electrically connected to the surface of the first side of the circuit board by wires. In order for the dice on both sides of the package to be electrically connected to one another, there must be connections present in the form of internal circuitry within the circuit board, as is conventional in the art. Swamy discloses an IC package in which the internal circuitry that is connected to the electrical conductor patterns on the exterior surfaces of the board are connected by vias (Fig. 3, col. 6, ln. 17-20). At the time of the

invention, it would have been obvious to one of ordinary skill in the art to form the inherent internal circuitry of conductive vias because it is well known in the art to provide vias in a substrate in order to connect circuitry on one surface of a circuit board to circuitry on the opposite surface of the board.

3. Claims 42 and 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiu in view of Swamy et al. and the admitted prior art.

Chiu does not disclose an input/output connector connected to the package. However, as stated above in reference to claims 32 and 44, an integrated circuit package must inherently have some form of an input/output connector in order to electrically access the attached semiconductor dice. Connectors such as a ball-grid array, a pin-grid array and socket connectors are conventionally used in the art. This is supported by the specification of the currently pending application which states on pg. 7, ln. 23-25 and pg. 8, ln. 14-15 that these types of connectors are "well known in the art". Swamy also discloses these three types of connectors to be conventional (col. 3, ln. 19-20; col. 4, ln. 4-7) and that each type of connector has offers its own advantages, and may be chosen depending upon the particular type of electrical component being connected to. In the invention of Chiu, a ball-grid array or pin-grid array connectors must be formed on the peripheral area of a circuit board because, as shown in Fig. 3, the peripheral area is the only surface of the board that is exposed (not covered with dice) and available for connectors to be attached thereto. In the case of using a socket type connector, this connector must also be formed on the edge of the board (also the peripheral area) for the same reasons. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use a

ball-grid array, a pin-grid array, or a socket connector located on the periphery of the substrate, to form the inherent input/output connectors of the package of Chiu because these types of connectors are well known and conventionally used in the art to connect IC packages to other electrical components.

4. Claims 41 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of Akram.

Chan shows in Figure 1 that the dice mounted to the first side of the circuit board are electrically connected to the surface of the second side of the circuit board by wires. The dice mounted to the second side of the circuit board are electrically connected to the surface of the first side of the circuit board by wires. In order for the dice on both sides of the package to be electrically connected to one another, there must be connections present in the form of internal circuitry within the circuit board, as is conventional in the art. Akram discloses a multichip package similar to that of Chan in which the internal circuitry that is connected to the electrical conductor patterns on the exterior surfaces of the board is specifically disclosed as being formed of vias (col. 3, ln. 58-61). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the inherent internal circuitry of conductive vias because it is well known in the art to provide vias in a substrate in order to connect circuitry on one surface of a circuit board to circuitry on the opposite surface of the board.

5. Claims 42 and 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. in view of Akram and Swamy and the admitted prior art.

Chan discloses an input/output connector of tabs (104) formed on the edge of the substrate which are used to mount the package vertically (col. 4, ln. 58-61). Chan does not disclose other types of connectors. As is disclosed by the specification of the currently pending application, socket connectors are also conventionally used to vertically mount packages, (pg. 8, ln. 14-15). Akram discloses a multichip IC package similar to that of Chan, in which the input/output connectors are formed of tabs in one embodiment, and are formed of a ball-grid array at the peripheral area of the board in another embodiment. Swamy discloses that socket connectors, ball-grid array connectors and pin-grid array connectors are all conventionally used in the art to form input/output connections to a circuit board of an IC package (col. 3, ln. 19-20; col. 4, ln. 4-7) and are used according to the type of electrical component being connected to. At the time of the invention, it would have been obvious to one of ordinary skill in the art to substitute a socket connector for the tabs of Chan because they are well known in the art for providing vertical connections to electrical components. It would also have been obvious to one of ordinary skill in the art to substitute either a ball-grid array or a pin-grid array for the tabs if the type of electrical component being connected to the board requires the board to be mounted horizontally instead of vertically because all of these types of connectors are conventional and well known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (703) 308-5840. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

CLN
July 30, 2001

Carl Whitehead Jr.

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800